

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Applicants: Vincent Dupaquis et al. PATENT APPLICATION

Serial No.: 10/615,476

Group Art Unit: 2124

Filed: July 7, 2003

For: COMBINED POLYNOMIAL AND NATURAL
MULTIPLIER ARCHITECTURE

Supplemental Information Disclosure Statement
with Certification under 37 CFR § 1.97(e)(1)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following information is submitted in compliance with Applicants' duty of disclosure under 37 CFR § 1.97(e). A copy of each of the cited references is enclosed.

OTHER REFERENCES

J. Garcia et al., *A Combined 16-Bit Binary and Dual Galois Field Multiplier*, IEEE Workshop on Signal Processing Systems, October 16, 2002, pages 63-68, XP-10616578.

W. Drescher et al., *VLSI Architectures for Multiplication in $GF(2^m)$ for Application Tailored Digital Signal Processors*, 1996 IEEE, pages 55-64, XP-000827643.

K.C. Bickerstaff et al., *Parallel Reduced Area Multipliers*, Journal of VLSI Signal Processing Systems, April 1995, Dordrecht, NL, pages 181-191, XP 000525881.

Luigi Dadda, *Composite Parallel Counters*, IEEE Transactions on Computers, Vol. C-29, No. 10, October 1980, pages 942-946, XP-000757822.

The undersigned hereby certifies that the items of information contained in this Supplemental Information Disclosure Statement were cited in a communication received from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

With respect to the Garcia paper, it does not qualify as prior art under 35 USC 102(b), nor does submission herewith constitute any admission that it would qualify as prior art under 35 USC 102(a) or any other subsection of 35 USC 102. Applicant is prepared to submit an affidavit or declaration under 37 CFR 1.131 if any claim is rejected on the basis of this paper.

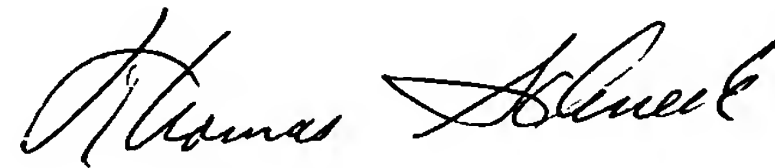
CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Signed: Brenda Elmidolan
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Date: April 9, 2004

Respectfully submitted,



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FORM PTQ-1449	Atty. Docket No. ATM-213	Serial No. 10/615,476
LIST OF PRIOR ART CITED BY APPLICANT	Applicants: Vincent Dupaquis et al.	
	Filing Date: July 7, 2003	Group: 2124



U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Publ. Date	Name	Class	Sub Class	Filing Date
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AD						
AE						
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AG						
AH						
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AJ						

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Document Number	Publ. Date	Country	Class	Sub Class	Translation Yes No
AK						
AL						
AM						
AN						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AO	J. Garcia et al., "A Combined 16-Bit Binary and Dual Galois Field Multiplier," IEEE Workshop on Signal Processing Systems, October 16, 2002, pages 63-38, XP-10616578.
AP	W. Drescher et al., "VLSI Architectures for Multiplication in GF (2 ^m) for Application Tailored Digital Signal Processors", 1996 IEEE, pages 55-64, XP-000827643.
AQ	K.C. Bickerstaff et al., "Parallel Reduced Area Multipliers", Journal of VLSI Signal Processing Systems, April 1995, Dordrecht, NL, pages 181-191, XP 000525881.

EXAMINER:

DATE CONSIDERED:

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